Amendments to the Specification:

Please replace the Abstract of the Disclosure with the following amended Abstract of the Disclosure:

~~A~~ In a Viterbi decoder, a ~~includes a branch metric calculating circuit, an adder-comparator-selector unit, a metric register, a survivor memory unit, a decision circuit, and optionally a normalizing circuit. For performing the decoding method, a plurality of target level sets are provided first. A~~ branch metric calculating operation of a series of received input data is performed according to ~~the~~ different sets of target levels to realize a plurality of branch metric values, wherein said target level sets are not identical. Accumulative operations of the branch metric values are performed, respectively, and the plurality of accumulated values are compared in groups. A plurality of control signals and a plurality of least accumulated values are outputted according comparing results of the accumulated values. The least accumulated values are received and stored, and then fed back for next accumulation operations. A plurality of possible output-data state transition tracks are recoded in response to the control signals. The output data are determined according to the least accumulated values and output-data state transition tracks.